Notice of Allowability	Application No.	Applicant(s)	
	10/719,878	BROWN ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *an amdt filed on 10/26/06*.

2. ☒ The allowed claim(s) is/are *1 and 3-20 (renumberd as 1-19)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and or additions be acceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no latter than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Charles Huston on 01/03/06.

2. The application has been amended as follows:

As per claim 16:

Line, 6 please change "a transition" to --- the transition---.

Examiner's statement for reason for allowance

3. Claims **1 and 3-20** have been allowed.

The following is an examiner's statement for allowance:

As per claim 1:

The prior of record, Vlahos (U.S. PN: 5,231,598) teaches or discloses a skew tester for testing output timing skew between multiple output signals of an integrated circuit (IC) device-under-test (DUT) having an input and multiple outputs (see col. 1, lines 6-9). Vlahos in figure 2 teaches that a DUT (25) pass through filters (28), signal splitting network (32), phase inverting amplifiers (34, 35) and selected for testing by a switch (44) applied to an input of comparator (exclusive OR gate) (45) and the output of

the comparator applied to a latch (50) (see col. 10, lines 15-36). The prior art of record, Langford, II (U.S. PN: 6,671,860) teaches a boundary scan
cell architecture and method for use to provide controllable fault injection in a system board under test (see col. 1, lines 9-13) and further in figure 4 Langford teaches an AND gate (403) receiving a signal_IN and the output the AND gate coupled to an XOR gate (400).

However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious an a logic gate placed within the functional path for receiving an output signal directly from the DUT on the one input of the logic gate and an expected output signal on another input of the logic gate absent any circuitry beyond the logic gate coupled for receiving the output signal and a latch placed within the functional path for receiving an output of the logic gate and forwarding the output of the logic gate from the latch into the bonding pad during times when the latch enters transparent mode. Consequently, claim 1 is allowed over the prior art.

Claims **3-7,** which is/are directly or indirectly dependent/s of claim 1 are also allowable over the prior art of record.

As per claim 8:

The prior of record, Vlahos (U.S. PN: 5,231,598) teaches or discloses a skew tester for testing output timing skew between multiple output signals of an integrated circuit (IC) device-under-test (DUT) having an input and multiple outputs (see col. 1, lines 6-9). Vlahos in figure 2 teaches that a DUT (25) pass through filters (28), signal splitting network (32), phase inverting amplifiers (34, 35) and selected for testing by a

switch (44) applied to an input of comparator (exclusive OR gate) (45) and the output of the comparator applied to a latch (50) (see col. 10, lines 15-36). The prior art of record, Langford, II (U.S. PN: 6,671,860) teaches a boundary scan
cell architecture and method for use to provide controllable fault injection in a system board under test (see col. 1, lines 9-13) and further in figure 4 Langford teaches an AND gate (403) receiving a signal_IN and the output the AND gate coupled to an XOR gate (400).

However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a first series-connected logic gate and latch coupled to receive a clock signal forwarded to the circuit, and to latch a transition of a clock signal, a second series-connected logic gate and latch coupled to receive an output signal from the circuit and an expected output signal, and to latch a transition of the output signal and a delay measurement device coupled to the output terminal for measuring the time difference between the transition of the clock signal and the transition of the output signal. Consequently, claim 8 is allowed over the prior art.

Claims **9-15,** which is/are directly or indirectly dependent/s of claim 8 are also allowable over the prior art of record.

As per claim 16:

The prior of record, Vlahos (U.S. PN: 5,231,598) teaches or discloses a skew tester for testing output timing skew between multiple output signals of an integrated circuit (IC) device-under-test (DUT) having an input and multiple outputs (see col. 1, lines 6-9). Vlahos in figure 2 teaches that a DUT (25) pass through filters (28), signal

splitting network (32), phase inverting amplifiers (34, 35) and selected for testing by a switch (44) applied to an input of comparator (exclusive OR gate) (45) and the output of the comparator applied to a latch (50) (see col. 10, lines 15-36). The prior art of record, Langford, II (U.S. PN: 6,671,860) teaches a boundary scan
cell architecture and method for use to provide controllable fault injection in a system board under test (see col. 1, lines 9-13) and further in figure 4 Langford teaches an AND gate (403) receiving a signal_IN and the output the AND gate coupled to an XOR gate (400).

However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a method of latching a transition of a clocking signal, latching a transition of the output signal and measuring the signal skew as a time difference between the transition of the clocking signal and when the transition of the output signal occurs. Consequently, claim 8 is allowed over the prior art.

Claims **17-20** which is/are directly or indirectly dependent/s of claim 16 are also allowable over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned (571) 273-8300.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Art unit: 2133

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